What is claimed is:

1. A method of manufacturing a SONOS flash memory device comprising the steps of:

forming a lower oxide layer, a tunnel nitride layer, a sacrificial oxide layer, and an insulating layer for a hard mask on a semiconductor substrate having device isolation regions;

removing a portion of the insulating layer for a hard mask by an etching process to expose a portion of the sacrificial oxide layer;

forming spacers on sidewalls of the insulating layer etched;

removing some part of the sacrificial oxide layer and the tunnel nitride layer by an etching process using the insulating layer and the spacers as a mask to expose a portion of the lower oxide layer;

removing the insulating layer, the spacers, and the sacrificial oxide layer;

removing a portion of the lower oxide layer by an etching process using the tunnel nitride layer etched as a mask to expose a portion of the substrate;

depositing an upper oxide layer and a polysilicon layer in sequence over the resulting structure; and

forming a gate having two separate tunnel nitride layer parts by removing some parts of the polysilicon layer, the upper oxide layer, and the tunnel nitride layer in sequence by an etching process.

2. The method as defined by claim 1, wherein the insulating layer for a hard mask is formed of oxide or nitride using tetraethyl orthosilicate (TEOS) as a source.

3. The method as defined by claim 1, wherein the spacers are formed of oxide or nitride using TEOS as a source.

4. The method as defined by claim 1 or claim 3, wherein the spacers are formed so that a space between the spacers is between 0.020 ㎛ and 0.5 ㎛.

5. The method as defined by claim 1, wherein a space between the two separate tunnel nitride layer parts is adjusted with a space between the spacers.